Efficiency Evaluation of Single-Phase Solutions for AC-DC PFC Boost Converters for Plug-in-Hybrid Electric Vehicule Battery Chargers

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***Abstract*— In this paper, the bridgeless interleaved boost topology is proposed for plug-in hybrid electric vehicle and electric vehicle battery chargers to achieve high efficiency, which is critical to minimize the charger size, charging time and the amount and cost of electricity drawn from the utility. An analytical model for this topology is developed, enabling the calculation of power losses and efficiency. Experimental and simulation results of prototype units converting the universal AC input voltage to 400 V DC at 3.4 kW are given to verify the proof of concept, and analytical work reported in this paper.**

Keywords-component; Boost Converter; Single phase PFC; Interleaved PFC; Bridgeless PFC; PHEV Charger;

I. INTRODUCTION

A plug-in hybrid electric vehicle (PHEV) is a hybrid vehicle with a storage system that can be recharged by connecting the vehicle plug to an external electric power source. In recent years, PHEV motor drive and energy storage technology has developed at a rapid rate in response to expected market demand for PHEVs. Battery chargers are another key component required for the emergence and acceptance of PHEVs. For PHEV applications, the accepted approach involves using an in-vehicle charger [1]. An in-vehicle 3.4 kW charger can charge a depleted battery pack in PHEVs to 95% charge in about four hours from a 240 V supply [2]. The accepted charger power architecture includes an AC-DC converter with power factor correction (PFC) [3] followed by an isolated DC-DC converter. Selecting the optimal topology and evaluating power losses in power semiconductors are important steps in the design and development of these battery chargers [4]. The front-end AC-DC converter is a key component of the charger system. In the following sub-sections, three common continuous conduction mode (CCM) AC-DC PFC boost converters are evaluated.

II. REVIEW OF EXISTING TOPOLOGIES

A. Conventional Boost Converter

The conventional boost topology is the most popular topology for PFC applications [5]. It uses a dedicated diode bridge to rectify the AC input voltage to DC, which is then followed by the boost section, as shown in Figure 1. In this topology, the output capacitor ripple current is very high [6, 7] and is the difference between diode current and the dc output current. Furthermore, as the power level increases, the diode bridge losses significantly degrade the efficiency, so dealing with the heat dissipation in a limited area becomes problematic. Due to these constraints, this topology is good for a low to medium power range up to approximately 1kW. For power levels >1kW, typically, designers parallel semiconductors in order to deliver greater output power. The inductor volume also becomes a problematic design issue at high power.

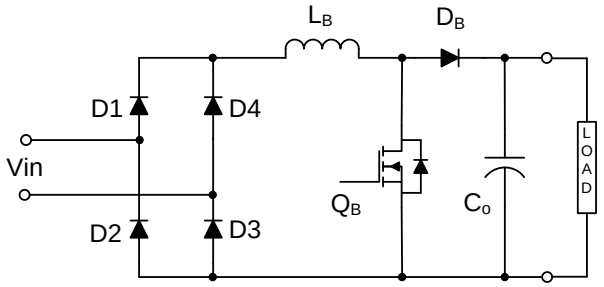

Figure 1: Conventional PFC boost converter

B. Bridgeless Boost Converter

The bridgeless boost converter topology [8-12] avoids the need for the rectifier input bridge, yet maintains the classic boost topology, as shown in Figure 2. It is an attractive solution for applications >1kW, where power density and efficiency are important. The bridgeless boost converter solves the problem of heat management in the input rectifier diode bridge, but it introduces increased EMI [13, 14].

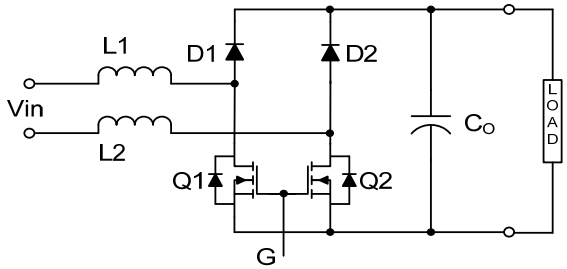

Figure 2: Bridgeless PFC boost topology

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Another disadvantage of this topology is the floating input line with respect to the PFC stage ground, which makes it impossible to sense the input voltage without a low frequency transformer or an optical coupler. Also in order to sense the input current, complex circuitry is needed to sense the current in the MOSFET and diode paths separately, since the current path does not share the same ground during each half-line cycle [9, 15].

C. Interleaved Boost Converter

The interleaved boost converter, Figure 3, is simply two boost converters in parallel operating 180° out of phase [16-18]. The input current is the sum of the two inductor currents I_{LB1} and I_{LB2}. Because the inductors' ripple currents are out of phase, they tend to cancel each other and reduce the input ripple current caused by the boost switching action. The interleaved boost converter has the advantage of paralleled semiconductors. Furthermore, by switching 180° out of phase, it doubles the effective switching frequency and introduces smaller input current ripples, so the input EMI filters will be smaller [19, 20]. It also reduces output capacitor high frequency ripple [21]. But it still has the problem of heat management for the input diode bridge rectifiers.

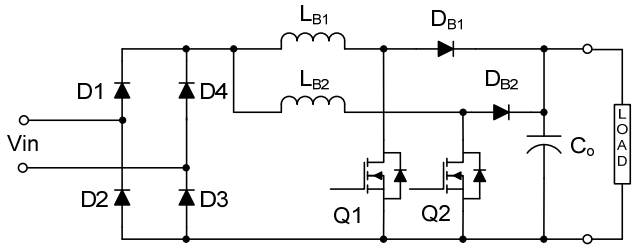

Figure 3: Interleaved PFC boost topology

III. Bridgeless Interleaved Boost Topology

The BLIL PFC shown in Figure 4 is proposed as a solution to problems addressed. Compared to the interleaved PFC converter, this topology introduces two more FETs and two more fast diodes in place of 4 slow diodes used in input bridge.

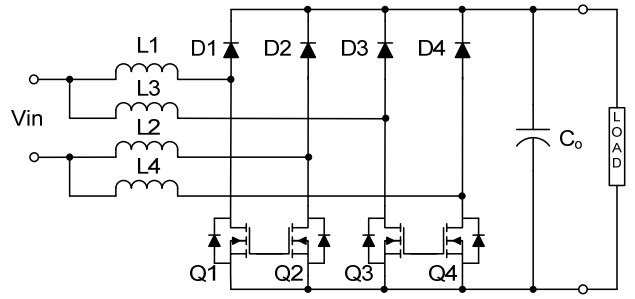

Figure 4: Bridgeless Interleaved PFC boost topology

To analyze the circuit operation, it has been separated into two half cycles. During the "positive" half cycle, when AC input voltage goes positive, Q1 turns on and current flows through L1, Q1 and continues through Q2 and then L2 to store energy in L1 and L2. When Q1 turns off, energy stored in L1 and L2 will be released as current flows through D1, through the Load and returns through the body diode of Q2 back to the mains.

The same cycle happens for Q3, but with a 180° phase delay. During the "negative" half cycle, Q2 and Q4 turn on, current flows through the inductors L2 and L1 (L4 and L3 for the interleaved one). When the MOSFETs are off, energy is released as current flows through D2 (and D4), through load and back to the main through the body diode of Q1 (and Q3). A detailed converter description is given in [22].

IV. Analytical Modelling

In order to properly select the power stage components of a converter and calculate the associated power losses, it is necessary to determine the RMS and average values of their currents. In a typical boost converter, the FET and diode current waveforms are pulsed-width modulated, with both the duty cycle and peak amplitude varying with the AC input. And without an effective mathematical method for computing these RMS and average values, the proper design and selection of power stage components can be flawed. The following assumptions were made in order to analyze the converters and to derive the stress equations:

a) These calculations are based on the operation of CCM PFC boost converter.

b) Assuming unity power factor, the line current is in phase and shape with the input line voltage – a sinusoidal waveform.

c) The PFC output voltage is DC with no voltage ripple.

In a typical boost converter, the converter FET duty cycle is given by:

$$\delta_Q(\theta) = 1 - \frac{|V_{in}(\theta)|}{V_o} = 1 - \frac{V_{in}|\sin(\theta)|}{V_o} \quad (1)$$

Assuming the inductor current is a sinusoidal waveform:

$$i_L = I_{PK}|\sin(\theta)| \quad (2)$$

The instantaneous FET current and its RMS current can be derived respectively:

$$i_Q = I_{PK}|\sin(\theta)|\left(1 - \frac{V_{PK}|\sin(\theta)|}{V_o}\right) \quad (3)$$

$$I_{Q-rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[I_{PK}|\sin(\theta)|\left(1 - \frac{V_{PK}|\sin(\theta)|}{V_o}\right)\right]^2 d\theta} \quad (4)$$

The inducotr current ripple is assumed to be half of peak inductor current:

$$\Delta I_{RP} = \frac{1}{2}\frac{I_{PK}}{2} \quad (5)$$

The high frequency ripple components of inductor current is assumed to be a triangler waveform with a fixed duty cycle, so the RMS current in each inductor is defined by:

$$I_{L-rms} = \sqrt{\left(\frac{1}{\sqrt{2}}\frac{I_{PK}}{2}\right)^2 + \left(\frac{1}{2\sqrt{3}}\Delta I_{RP}\right)^2} = \frac{5}{4\sqrt{3}}\frac{P_{in}}{V_{PK}} \quad (6)$$

TABLE I. SUMMARY OF COMPONENT RMS CURRENT STRESS FOR CONVENTIONAL BOOST AND BRIDGELESS BOOST TOPOLOGIES

Topology	Conventional PFC	Bridgeless PFC
Boost Inductor	$\sqrt{\frac{97}{48}}\frac{P_{in}}{V_{PK}}$	$\sqrt{\frac{97}{48}}\frac{P_{in}}{V_{PK}}$
Input Bridge Diode	$\frac{P_{in}}{V_{PK}}$	Not Applicable
Boost Fast Diode	$\sqrt{\frac{3}{2}}\frac{P_{in}}{V_o}$	$\frac{\sqrt{3}}{2}\frac{P_{in}}{V_o}$
Boost Transistor	$\frac{P_{in}}{\sqrt{6}V_{PK}V_o}\sqrt{\frac{3\pi(3V_{PK}^2+4V_o^2)-64V_{PK}V_o}{\pi}}$	$\frac{P_{in}}{\sqrt{6}V_{PK}V_o}\sqrt{\frac{3\pi(3V_{PK}^2+4V_o^2)-64V_{PK}V_o}{\pi}}$
Boost Transistor Intrinsic Diode	Not Applicable	$\frac{\sqrt{3}}{2}\frac{P_{in}}{V_o}$
Output Capacitor Ripple (LF)	$\frac{\sqrt{2}}{2}\frac{P_o}{V_o}$	$\frac{\sqrt{2}}{2}\frac{P_o}{V_o}$
Output Capacitor Ripple (HF)	$\frac{\sqrt{2}}{2V_o}\sqrt{3P_{in}^2-2P_o^2}$	$\frac{\sqrt{2}}{2V_o}\sqrt{3P_{in}^2-2P_o^2}$

TABLE II. SUMMARY OF COMPONENT CURRENT STRESS FOR INTERLEAVED AND BRIDGELESS INTERLEAVED BOOST TOPOLOGIES

Topology	Interleaved PFC	Bridgeless Interleaved PFC
Boost Inductor	$\frac{5}{4\sqrt{3}}\frac{P_{in}}{V_{PK}}$	$\frac{5}{4\sqrt{3}}\frac{P_{in}}{V_{PK}}$
Input Bridge Diode	$\frac{P_{in}}{V_{PK}}$	Not Applicable
Boost Fast Diode	$\sqrt{\frac{3}{2}}\frac{P_{in}}{2.V_o}$	$\frac{\sqrt{3}}{4}\frac{P_{in}}{V_o}$
Boost Transistor	$\frac{P_{in}}{2\sqrt{6}V_{PK}V_o}\sqrt{\frac{3\pi(3V_{PK}^2+4V_o^2)-64V_{PK}V_o}{\pi}}$	$\frac{P_{in}}{2\sqrt{6}V_{PK}V_o}\sqrt{\frac{3\pi(3V_{PK}^2+4V_o^2)-64V_{PK}V_o}{\pi}}$
Boost Transistor Intrinsic Diode	Not Applicable	$\frac{\sqrt{3}}{4}\frac{P_{in}}{V_o}$
Output Capacitor Ripple (LF)	$\frac{\sqrt{2}}{2}\frac{P_o}{V_o}$	$\frac{\sqrt{2}}{2}\frac{P_o}{V_o}$
Output Capacitor Ripple (HF)	$\frac{P_{in}}{V_o}\sqrt{\frac{16\,V_o}{6\pi\,V_{PK}}-1.5\frac{P_o^2}{P_{in}^2}}$	$\frac{P_{in}}{V_o}\sqrt{\frac{16\,V_o}{6\pi\,V_{PK}}-1.5\frac{P_o^2}{P_{in}^2}}$

The boost diode duty cycle is given by:

$$\delta_D(\theta) = 1 - \delta_Q(\theta) = \frac{V_{PK}|\sin(\theta)|}{V_o} \quad (7)$$

Therefore the instantaneous boost diode current and its RMS current can be derived respectively:

$$i_D = I_{PK}|\sin(\theta)|\frac{V_{PK}|\sin(\theta)|}{V_o} \quad (8)$$

$$I_{D-rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[I_{PK}|\sin(\theta)|\left(\frac{V_{PK}|\sin(\theta)|}{V_o}\right)\right]^2 d\theta} \quad (9)$$

The output capacitor current has high frequency and low frequency components. The low frequency component is simply calculated by:

$$I_{C-rms(LF)} = \frac{I_o}{\sqrt{2}} = \frac{\sqrt{2}}{2}\frac{P_o}{V_o} \quad (10)$$

And the high frequency RMS ripple current component is:

$$I_{C-rms(HF)} = \frac{P_{in}}{V_o}\sqrt{\frac{16\,V_o}{6\pi\,V_{PK}}-1.5\frac{P_o^2}{P_{in}^2}} \quad (11)$$

The same method was used to derive RMS current in different topologies. Table 1 shows a summary of component

RMS current stress for conventional boost converter and bridgeless boost converter. Table 2 provides the same summary for interleaved boost converter and bridgeless interleaved boost converter.

As can be noted, in both the bridgeless topology and bridgeless interleaved topology, a new loss has been introduced in the intrinsic body diodes of the FETs, but since input bridge rectifiers were eliminated, there is some efficiency gain in overall performance of these topologies. The intrinsic body diode of FETs conduct when the boost transistors are off and its value is the same as the current in the boost diodes, when they conduct and transfer energy to the output capacitors.

Also the low frequency RMS ripple current through output capacitors is constant and interleaving has no effect on it. But the high frequency ripple current will be reduced significantly, as it is shown in Figure 5. Also it is noted that as the input voltage increases, the high frequency ripple reduces.

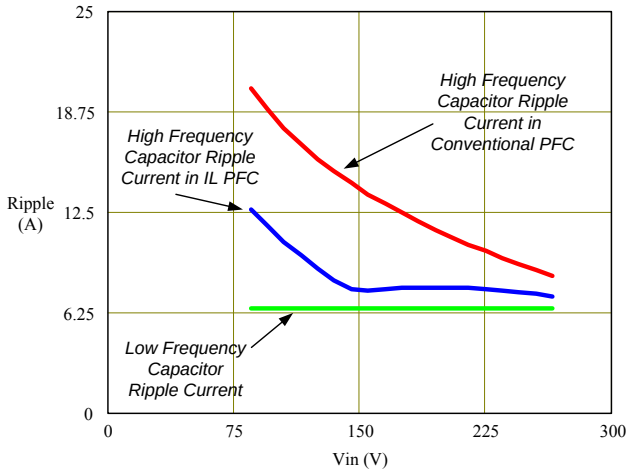

Figure 5: RMS ripple current through output capacitors vs input voltage

V. Loss Evaluation

Figure 6 shows the loss distribution of the semiconductors in the four topologies investigated in this paper. The regular diodes in input bridge rectifiers have the largest share of losses among the topologies with the input bridge rectifier. The bridgeless topologies eliminate this large loss component (~30W). However, the tradeoff is that the FET losses are higher and the intrinsic body diodes of FETs conduct, producing new losses (~8W). The fast diodes in the conventional and interleaved PFC have slightly lower power losses, since the boost RMS current is higher in these topologies. Overall the FETs are under more stress in bridgeless topologies, but the total loss for the proposed bridgeless interleaved boost are 40% lower than the benchmark conventional boost, 27% lower than the bridgeless boost and 32% lower than the interleaved boost .

Since the bridge rectifier losses are so large, it was expected that bridgeless interleaved boost converter would have the least power losses among all four introduced topologies. Also it was noted that the losses in the input bridge rectifiers were 63% of total losses in conventional PFC converter and 71% of total losses in interleaved PFC converter. Therefore eliminating the input bridges in PFC converters is justified despite the fact that new losses are introduced.

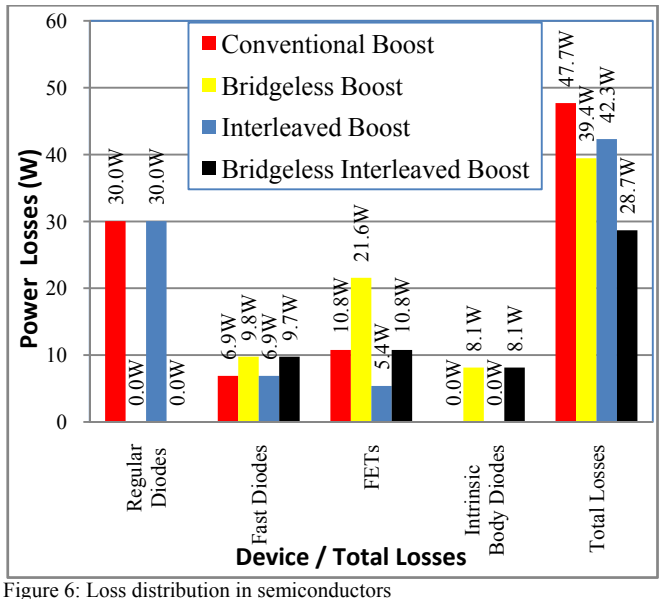

Figure 6: Loss distribution in semiconductors

VI. Experimental Results

A prototype of the bridgeless interleaved converter circuit was built to verify proof-of-concept and analytical work presented in this paper as shown in Figure 7. The performance was compared with a benchmark interleaved boost converter.

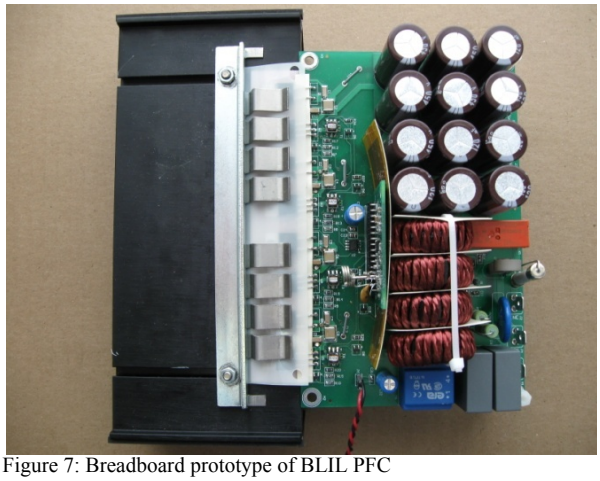

Figure 7: Breadboard prototype of BLIL PFC

Table 3 shows the semiconductors and power components used in the 3.4 kW CCM experimental prototypes – an interleaved boost PFC converter and a bridgeless interleaved PFC converter. The prototypes were built for a universal ac-line input (85~265 V) RMS at 400 V output.

Figures 8 to 11 show the converter efficiency versus output power for the interleaved boost PFC converter and bridgeless interleaved boost PFC converter at input voltages of 240V, 220V, 120V and 90V and the following test conditions: f_{sw} = *70 kHz*, I_{in_max} = *15 A* and V_o = *400 V*. Since the maximum full load input current is kept constant at 15 A, the output power varries from 1200 W for 90 V input, 1.7 kW for 120 V input, 3 kW for 220 V input and 3.4 kW for 240 V input voltage. Maintaining a maximum input current limit is required for

residential charging applications to ensure a 20A breaker is not tripped.

With the proposed bridgeless interleaved PFC converter a peak efficiency of 98.2% was reached at 240 V input and 1 kW output power (Figure 8). This represents a 1% improvement compared to the interleaved PFC converter. Furthermore, at lighter loads, especially at low input lines, converter efficiency is improved significantly (as high as 3% at 200 W) compared to interleaved boost converter.

As illustrated in Figure 11, at 90V input, the peak efficiency of the interleaved bridgeless PFC is 95.8% at 400 W, which is slightly lower than high line input, as expected. This compares to a 94.8% efficiency for the interleaved PFC.

TABLE III. DEVICES/COMPONENTS USED IN PROTOTYPE UNITS

Topology	Device	Part # / Value	# of devices
Interleaved PFC	Regular Diode	25ETS08S	4
	Fast Diode	IDB06S60C	2
	MOSFET	IPB60R099CP	2
	Inductor	800 µH	2
Bridgeless Interleaved PFC	Fast Diode	CSD10060	4
	MOSFET	IPP60R099CP	4
	Inductor	400 µH	4

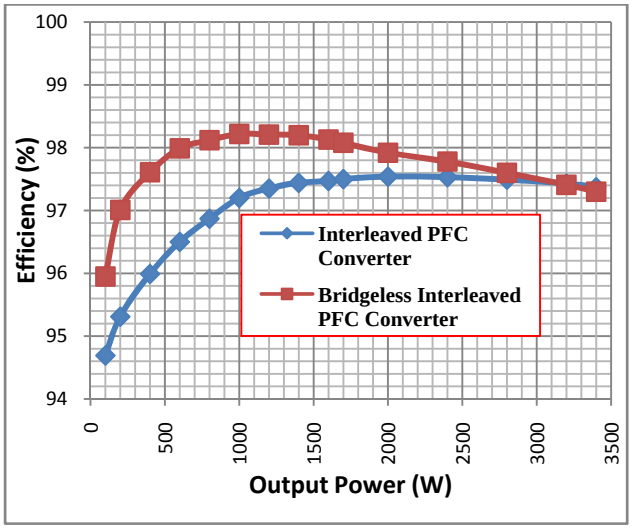

Figure 8: Efficiency vs. output power for Interleaved and Bridgeless Interleaved PFC Boost Converter at Vin = 240 V

A Yokogawa W230 digital power meter was used for efficiency measurements. A Chroma 63202 DC electronic load and an Agilent 6834B AC source/Analyzer were also used in the experiments.

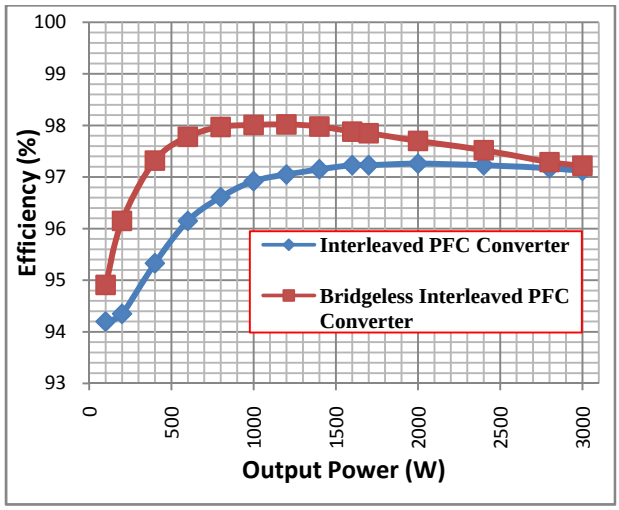

Figure 9: Efficiency vs. output power for Interleaved and Bridgeless Interleaved PFC Boost Converter at Vin = 220 V

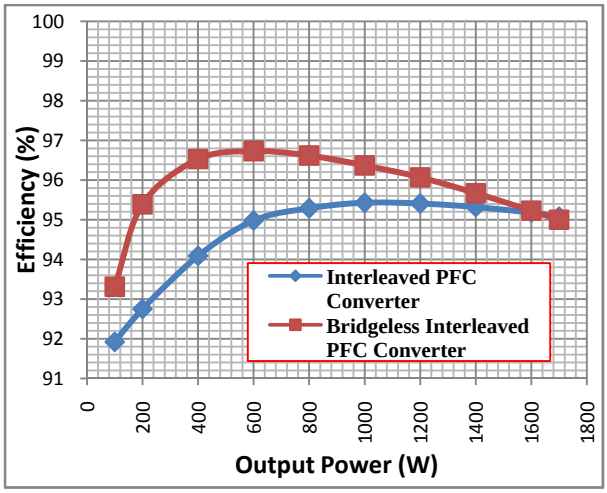

Figure 10: Efficiency vs. output power for Interleaved and Bridgeless Interleaved PFC Boost Converter at Vin = 120 V

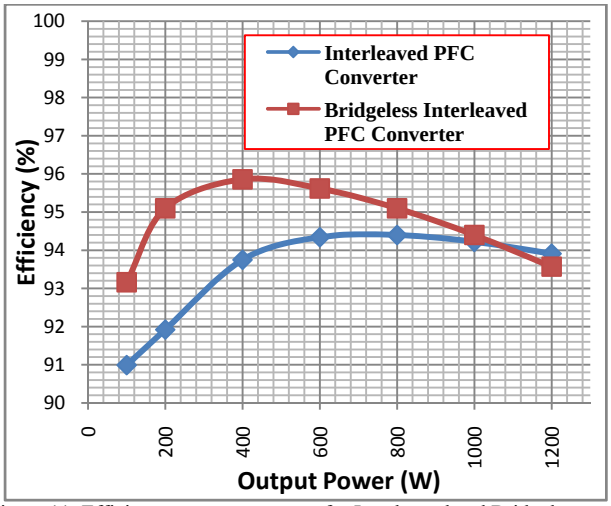

Figure 11: Efficiency vs. output power for Interleaved and Bridgeless Interleaved PFC Boost Converter at Vin = 90 V

VII. Conclusion

A new high efficiency bridgeless interleaved PFC AC-DC Boost converter topology has been presented in this paper. The target application for the converter is the front-end AC-DC converter in plug-in hybrid electric vehicle battery chargers. The proposed converter has been analyzed and its performance characteristics have been presented. Also an analytical model for four different topologies was developed, enabling the calculation of power losses and efficiency calculation. A breadboard converter circuit has been built to verify the proof-of-concept. The proposed converter achieves a peak efficiency of 98.2 %, which represents a 1% improvement compared to the conventional interleaved PFC benchmark. The proposed converter achieves significantly improved efficiency up to full load across a wide input range of 90-240V.

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