A Novel Voltage Balance Method for Cascaded H-Bridge Rectifier

Tao Xinghua[1,2], Li Yongdong[1], Sun Min[1]
[1]Dept. of Electrical Engineering, Tsinghua University, China
[2] Dept. of Electrical Engineering, Naval Engineering University, China
E-mail: taoxh06@mails.tsinghua.edu.cn

Abstract—**In this paper, a novel algorithm is introduced for DC-link voltage balancing in cascaded H-bridge rectifier. With this method, the modulation index of each cell can be regulated by surveying not only the total DC voltage but also each cell's DC voltage, therefore the modulation index of each cell can match their individual actual active power respectively and achieve the DC voltages balance. Furthermore, the steady area of such cascaded converter is discussed and the relationship of the active power ratio of two cells and the modulation index is given. Simulation and experimental results show the proper operation of the proposed topology and the corresponding control strategy.**

***Keyword*—Voltage balance method; transformerless; cascaded H-bridge converter**

I. INTRODUCTION

Multilevel converters are attracting more and more interest in recent years due to its applications in high voltage situations such as active power filter and locomotive traction [1, 2]. Among the possible topologies of multilevel converters, cascaded H-bridge (CHB) topology is of particularly interest for its modular structure, easy implementation and less components [3, 4]. Moreover, it can reduce the voltage stress of the power switches and the size of the filter elements on the output of the inverter. Compared to the CHB inverter, the CHB rectifier is more attractable because it can provide several dc sources with a single high voltage ac input voltage. Especially in high voltage drive system the CHB rectifier can be connected directly to the grid, hence the transformer can be eliminated and the volume is reduced.

The structure of the CHB rectifier is shown in the dashed line in Fig.1 and several H-bridge rectifiers can be connected in cascade. As all cascaded cells have the same current, only one current controller is needed to regulate the output DC voltage, thus it is difficult to balance the output DC voltage of rectifiers when they feed different loads. In [5] a PI-based controller for a two-cell CHB is discussed and the proposed solution consist of one PI for the total DC-link voltage, one PI for a DC-link voltage and one P for current. With such method DC-link voltages balance can be achieved, though it is difficult to design the PI controller when the number of cell is larger than two. To make controller more simple, reference [6] proposed another solution. The voltage balance is controlled by a digital controller, with only one cell keeps in PWM state and the others in either charging or discharging state during one switching period. So, it needs no special PI for DC-link voltage balance. In [7], the inherent stability problem of such topology is concerned and passivity-based controller is introduced. Though oscillatory state can be avoided, more calculation is needed, the control method becomes complex greatly.

Reference [8] gives a simple method for voltage balancing. Although the cascaded H-bridge topology mentioned above is used in the active filter application and no active power is delivered from the converter contrast to the CHB rectifier, the voltage balance strategy is still useful. In this paper, the similar method is applied into CHB rectifier. First, the impact on the output voltage by modulation index bias is considered; then the relationship between the difference of DC-link voltage and modulation index bias is deduced; finally the control scheme is discussed in detail. For simplicity, only two-cell CHB topology is considered, and the method can be easily extended to more levels.

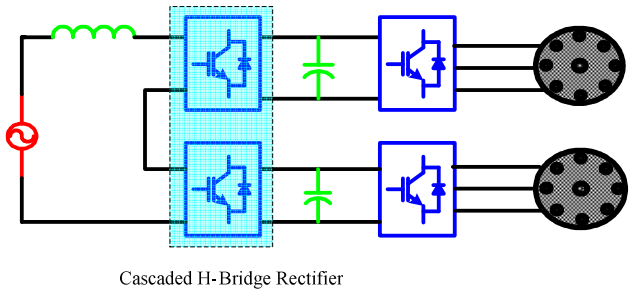

Fig.1 Two-cell CHB rectifier in the multi-motor drive system

II. MATHMETICSAL MODEL OF THE SYSTEM

The considered two-cell rectifier is shown in Fig.1. With the help of the switch function S_1, S_2, the two-cells CHB rectifier can be completely described by a group of differential equations:

$$u_s - L_s \frac{di_s}{dt} = S_1 u_{dc1} + S_2 u_{dc2} = u_{afe}$$

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$$C_1 \frac{du_{dc1}}{dt} = S_1 i_s - \frac{u_{dc1}}{R_1}$$

$$C_2 \frac{du_{dc2}}{dt} = S_2 i_s - \frac{u_{dc2}}{R_2}$$

Where u_s, i_s are the grid voltage and current;

u_{afe}, u_{dci} are the ac side and dc side voltages of rectifier;

L_s is the AC inductance.

C_1, C_2 and R_1, R_2 are each cell's DC bus capacitor and load resistors.

The switching functions S_i ($i = 1, 2$) is defined with the state of power switchs T (1 for open, 0 for close) as following:

$$S_i = T_{i1} * T_{i4} - T_{i2} * T_{i3}$$

Considering one control period T_s, applying the moving average operator $\frac{1}{T_s}\int_t^{t+T_s} x(t)dt$ to the switching model above, thus resulting in

$$\overline{u}_s - L_s \frac{d\overline{i}_s}{dt} = d_1 \overline{u}_{dc1} + d_2 \overline{u}_{dc2}$$

$$C_1 \frac{d\overline{u}_{dc1}}{dt} = d_1 \overline{i}_s - \frac{\overline{u}_{dc1}}{R_1} \quad (1)$$

$$C_2 \frac{d\overline{u}_{dc2}}{dt} = d_2 \overline{i}_s - \frac{\overline{u}_{dc2}}{R_2} \quad (2)$$

In the average model, the switching functions S_1, S_2 are replaced by modulation index d_1, d_2 .It brings some convenience in discussing the controller for the following sections.

III. THE PRESENTED ALGORITHUM

A. *The main control structure*

The CHB rectifier is designed to operate at unity power factor. Because of the series structure, all cells have the same current. It means that only one current regulator is necessary. At the same time, the series rectifiers can be seen as an entire one from the AC side. Then, the control scheme of CHB rectifier can be divided into two parts: one is to shape the input AC current waveform and regulate the total DC voltages of all cells while the other one is to balance the DC voltage of each cell.

The first part of control scheme, which is familiar as the usual single-phase rectifier, is shown in Fig. 2. In a classic control structure, two main controllers $G_v(s)$ and $G_i(s)$ are employed [9, 10]. The total dc-link voltage is measured and then compared to the reference voltage value. The error is regulated by a PI controller $G_v(s)$. As the DC-link voltage waveform is composed of a constant value plus a double-time grid frequency component because of the pulsing power flowing to the cell, a low pass filter is required when sampling the DC voltage [11]. In order to obtain unity power factor, the output of $G_v(s)$ is multiplied by the grid voltage to generate the current reference. In the current loop, a PR (proportional and resonant) controller $G_i(s)$ is used to regulate the sinusoidal grid current. Because of the large open loop gain at the grid frequency, PR controller can eliminate the error between the current reference and the actual current. The output of the PR controller is the modulation index d . It is obvious that d stands for the total voltage reference of the CHB rectifier. In order to get the voltage of each cell, the following voltage balance algorithm is necessary.

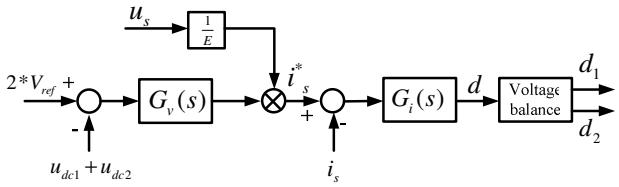

Fig.2 The main control structure of CHB rectifier

B. *Voltage balance algorithm*

Compared to the active filter, CHB rectifier mainly delivers active power. Therefore, the unbalanced active power between cells can result the DC-link voltage unbalance. In (1) ~ (2), the capacitor values of different cells are chosen to be the same. However the load resistors' values R_1, R_2 are not always the same, thus resulting in different modulation indexes d_1 and d_2 .Then the aim of achieving equal DC voltages becomes the job to distribute the total modulation index to the two cells. It is apparently that when the modulation indexes d_1, d_2 match the output active power of the cells respectivelly, the DC-link voltage can be balanced in the steady state.

From the above statement, the DC-link voltage balance law can be obtained. When load resistors values R_1, R_2 are same, the two cell modulation index d_1, d_2 are same as well. That is

$$d_1 = d_2 = \frac{d}{2}$$

If $R_1 \neq R_2$, the output active powers of cells are different. Then we have $d_1 \neq d_2$. It means that the total modulation index d should be rearranged in the cells. Different distribution methods result in different voltage balance methods. Obviously when d_1 is larger than $d/2$ d_2 must be smaller than $d/2$ because the sum of d_1, d_2 always equals to d and vice versa. If the biases between the cells can be solved, the voltage balance will be achieved.

In one control period, the total index d is kept in constant when d_1 and d_2 is rearranged so as to regulate the

current and the sum of dc link voltages. The equation can be derived as follows:

$$d_1 u_{dc1} + d_2 u_{dc2} = d \times 2V_{ref} \tag{3}$$

$$(d_1 + \Delta d_1)u_{dc1} + (d_2 + \Delta d_2)u_{dc2} = d \times 2V_{ref} \tag{4}$$

Where Δd_1、Δd_2 are the bias of d_1 and d_2.

V_{ref} is the DC-link voltage reference.

To get the bias required, the relationship between the DC-link voltage and the modulation index must be investigated. For convenience, the following derivation does not contain any subscripts because it is applicable for any of the cells.

According to the average model (1), when the current controller outputs the modulation index d in one control period time T_s the increment of the DC-link voltage can be shown as:

$$\begin{aligned}\Delta u_{dc} &= \frac{1}{C}(i_s - i_L)dT_s - \frac{1}{C}i_L(1-d)T_s \\ &= \frac{1}{C}T_s(i_s d - i_L)\end{aligned} \tag{5}$$

Where i_L is the load current.

The load current changes littlely in a short control period T_s, so it can be regarded as constant. Applying the equation (3) again, another DC voltage increment $\Delta u_{(d+\Delta d)}$ can be calculated with the modulation index $d + \Delta d$. Then the effect of the modulation index bias Δd to the DC-link voltage can be deduced as

$$\Delta V_{dc} = \Delta u_{(d+\Delta d)} - \Delta u_{(d)} = \frac{T_s}{C}\Delta d \times i_s \tag{6}$$

Assuming that the voltage balance is achieved in one control interval T_s, the following formula can be satisfied:

$$V_{dc1} + \Delta V_{dc1} = V_{dc2} + \Delta V_{dc2} \tag{7}$$

From (3)~(7), the bias would be calculated as:

$$\Delta d_1 = \frac{f_s C}{i_s}\frac{(u_2 - u_1)u_2}{(u_1 + u_2)} \tag{8}$$

$$\Delta d_2 = \frac{f_s C}{i_s}\frac{(u_1 - u_2)u_1}{(u_1 + u_2)} \tag{9}$$

Clearly, the modulation index bias is related to many variables: switching frequency, capacitance, grid current and the difference between DC-link voltages.

After the biases are solved, the actual modulation signal d_1、d_2 can be derived as follows:

$$d_1 = \frac{d}{2} + \Delta d_1$$

$$d_2 = \frac{d}{2} + \Delta d_2$$

When the method is put into practice, there are two problems which should be solved. The first is that when $i_s = 0$, the modulation index bias Δd will be equal to infinite, which must be avoided. The other one is that the polarity of the current can not be sampled accurately with the high frequency disturbance when the current is near zero. With the disturbance, wrong control signal will be given by (8), (9).

To solve above problems, approximation is taken. Note that the amplitude of current only decides the track speed [4] while the polarity of current will decide the polarity of control signal. The later one is more important during control, so one variable ξ, which has the same polarity with current, is used to replace the current. Since the current will keep in step with the grid voltage when the system is in steady state, ξ should has the following form

$$\xi = \cos(\omega t + \theta_u)$$

The modulate index bias can be written as

$$\Delta d_i \propto K\xi(\frac{1}{n}\sum_{k=1}^{n} u_k - u_i)$$

Where constant $K = Cf_s$.

According to above approximation, the final control structure is shown in figure3.

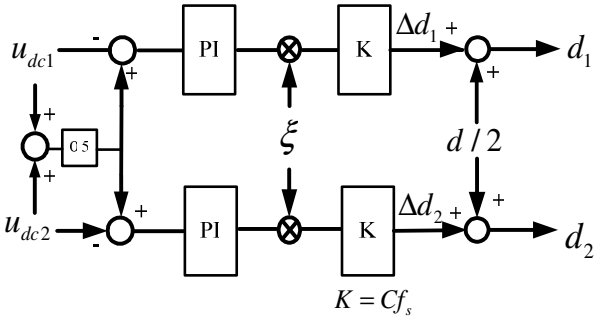

Fig.3 The proposed control scheme

C. The stability range of the system

As the modulation index bias Δd regulates the DC-link voltage by modulating the output active power of cell match the cell's modulate index d, the amplitude of d will be propotion to that cell's output active power. Thus considering the two cell CHB rectifier, modulation indexes and output powers should satisfy the equation below when the system keep in steady state:

$$d_{1A} : d_{2A} = P_1 : P_2 \tag{10}$$

Where d_{1A}, d_{2A} are the amplitude of d_1 and d_2.

P_1, P_2 are the active power of each cell.

Define active power ratio k

$$k = \frac{P_1}{P_2} > 0$$

The equation can be easily deduced:

$$\begin{cases} k \le \dfrac{1}{d-1} & k > 1 \\ k \ge d - 1 & 0 < k \le 1 \end{cases} \tag{11}$$

Fig.4 demostrates that the possible range of the active power ratio can be very large at low modulation index theoretically. As the total index d increases, the

probably range of k will become nerrow. The modulation index is decided by the DC-link voltage reference when the grid voltage keeps constant. Therefore, when designing such CHB rectifer feeding different loads, the DC-link referencce voltage must be selected by the probable active power ratio. Otherwise, steady state maybe not reach when the rectifier is working.

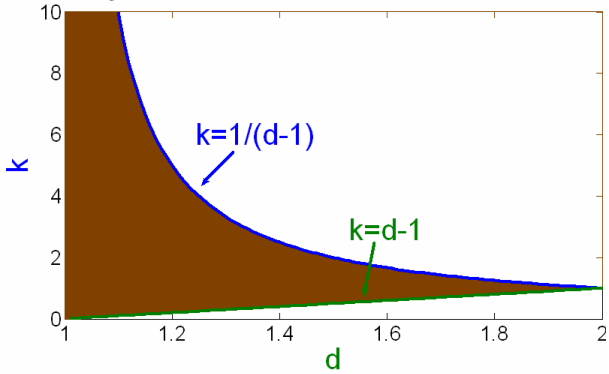

Fig.4 Steady operating area of CHB rectifier

IV. SIMULATION AND EXPERIMENTAL RESULTS

Using the presented method, some simulation tests have been performed adopting 5K Hz switching frequency. Fig.5 shows the transition of two cells' DC-link voltage due to two load step changes. Fig.6 is the waveforms of two modulate indexes with load step changes twice (at $t = 0.2s$ and $t = 0.5s$). It is clear that the indexes of two cells are rearranged automatically to match the output active power when load changes occur. The change of modulation indexes lead to balanced DC-link voltages.

To verify the feasibility of the proposed algorithm moreover, a prototype laboratory model of two-cell CHBR is made using MITSUBISHI IPM Type PM50RVA120. The controller is made up of TMS320F28335DSP chip. The parameters of the prototype are reported in Table.1.

TABLE I
Electrical parameters of the system

Peak grid voltage	100	V
DC-link voltage reference	60	V
AC inductance	7.5	mH
DC capacitors	2350	uF

Five steps are included in the experiments as following:

Step1: no load operating; ($R_1 = R_2 = 100K\Omega$)

Step2: with two equal loads; ($R_1 = R_2 = 28\Omega$)

Step3: with two different loads ($R_1 = 14\Omega; R_2 = 28\Omega$)

Step4: from step3 to step2; ($R_1 = R_2 = 28\Omega$)

Step5: from step2 to step1; ($R_1 = R_2 = 100K\Omega$)

Fig.7 shows the entire experimental process. The top waveform is the grid current. The change in its amplitude demonstrates the load steps in the experiment. The bottom waveforms are the measurement of the DC-link voltages. They can be kept at the reference value in the steady state. Fig.7 proves the effective of the proposed method.

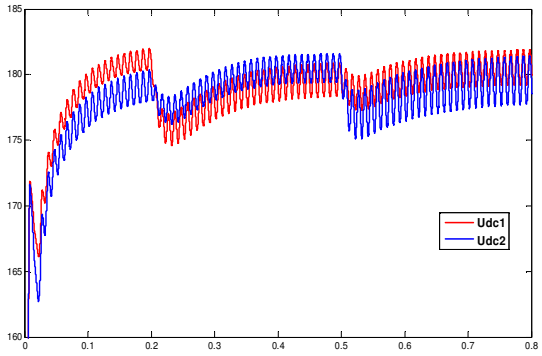

Fig.5 DC bus voltage waveform of two power cells

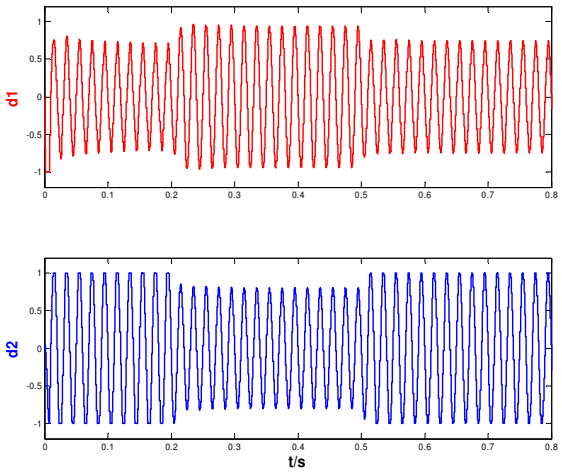

Fig.6 Modulate index d_1, d_2 with two load steps change

Fig.8 illustrates the grid voltage and current in the step 4, in which the total active power of system is decreased. As a result, the amplitude of grid current is decreased too. During the whole period, the current keeps well in phase with the grid voltage. It is shown that the current regulator has a good performance.

Fig.9 reports the DC-link voltages' transition of step 4 in detail. When the load of cell one (R_1) becomes little suddenly, the balance DC voltages stray the previous states. The voltage value of cell one increases. However, with the function of the controller the DC-link voltages are regulated to the reference value with some control periods. It demonstrates that the proposed voltage balance method is effective.

Fig.10 is the AC side PWM voltage. Due to the phase-shift PWM method is used, the voltage is a 5-level waveform. It can eliminate higher order harmonic components and then improve the grid current performance.

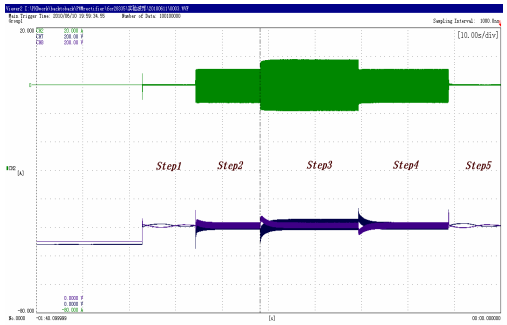

Fig.7 Measured grid current (10 A/div) and capacitance voltage (20 V/div)

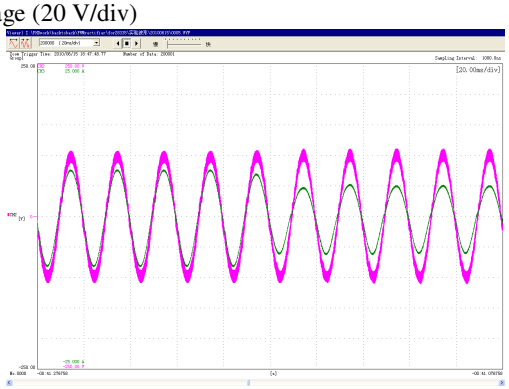
Fig.8 Measured grid voltage (50 V/div) and current(10 A/div).

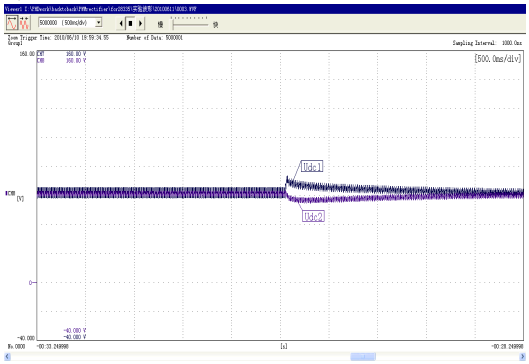

Fig.9 Measured DC-link voltages (20 V/div) due to one of the load step change

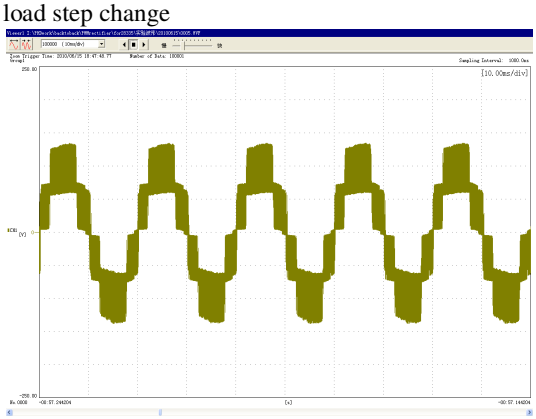
Fig.10 Measured AC side voltage (50 V/div) in five periods

V. CONCLUSIONS

Voltage balancing in cascaded H-bridge rectifier is not easy to achieve when the load of each cell is not equal. In this paper, a DC-link voltage balancing algorithm is proposed. The method is based on rearranging the modulation index of each individual cell so that the output power of each cell can be regulated to match the expected power respectively. Simulation and experimental results verify that with the proposed method, DC voltages keep balanced with non-equal loads.

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