A DSP Digital Controller Design and Implementation of High Power Boost Converter in Hybrid Electric Vehicles

Omar Ellabban, *Student Member, IEEE*, Omar Hegazy, *Student Member,IEEE*, Joeri Van Mierlo and Philippe Lataire

***Abstract*- This paper presents a DSP based direct digital control (DDC) design and implementation for a high power boost converter. A dual loop voltage control is digitally implemented using DSP. The real time workshop (RTW) is used for automatic real-time code generation. A laboratory prototype of a 20 kW boost converter based on TMS320F2808 DSP is presented. The proposed controller performance is investegated using MATLAB simulation and laboratory experments during reference voltage changes, input voltage changes, and load disturbances. Simulation and expermental results verify the efficacy of the proposed controller. In addition, the experimental results validate the effectiveness of using the RTW for automatic code generation to speed up the system implementation**.

Index Terms-Boost converter, digital signal processor (DSP), direct digital control (DDC), real time workshop (RTW).

I. INTRODUCTION

With increasing oil price and global warming, automobile manufacturers are producing more hybrid electric vehicles (HEV) and electrical vehicles (EV). Many research efforts have been focused on developing efficient, reliable, and low-cost power conversion techniques for the future new energy vehicles.

Fuel Cell Hybrid Electric Vehicle (FCHEV), as shown in Fig. 1, utilizes a fuel cell as the main power source and energy storage system (e.g. batteries, supercapacitors) as the auxiliary power source to assist the propulsion of the vehicle during transient and to absorb the kinetic energy during regenerative braking. In this topology, the FC is connected to the DC Bus via a boost converter and the energy storage system is connected to the DC Bus via a bidirectional converter [1].

The design of high power DC-DC converters and their controller plays an important role to control power regulation particularly for a common DC bus. Several such topologies of DC-DC converters based on their components count, advantages and disadvantages are discussed and compared in [2-4]. The boost converter offers higher efficiency and less component counts compared to other DC-DC converters topologies, which could possibly be used to interface fuel cell system to the load, so that it can be widely applicated in HEV.

Digital control of DC-DC power converters is becoming more and more common in industry today because of the availability of low cost, high performance Digital Signal Processing (DSP) controller with integrated power electronic peripherals such as analog to digital (A/D) converters and pulse width modulator (PWM). DSP based digital control allows the implementation of more functional control schemes, standard control hardware design for multiple platforms and flexibility of quick design modifications to meet specific customer needs.

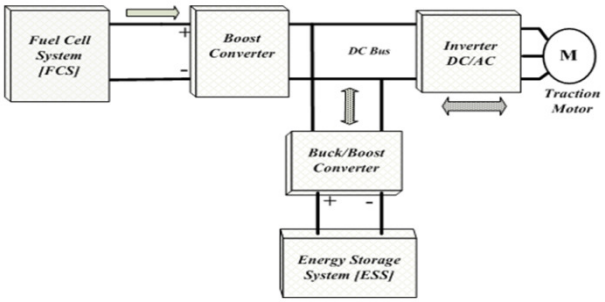

Fig. 1 The block diagram of FCHEV

Digital controllers are less susceptible to aging and environmental variations and have better noise immunity [5].

Computer Aided Control System Design (CACSD) tools are extensively used to generate real time code automatically. The graphical programming approach removes the need to write software by hand and allows the engineer to focus instead on improving functionality and performance. Complete system design is carried out within the simulation environment [6]. One of the DSP development tools which produces code directly from block set models is the real time workshop (RTW) for use with MATLAB and Simulink. It automatically builds programs that can be run in a variety of environments, including real time systems and stand alone simulations. The RTW allows rapid prototyping, a process that conceptualizes solutions using a block diagram modeling environment. It reduces algorithm coding to an automated process, which includes coding, compiling, linking, and downloading to the target processor [7].

There are two approaches to design a digital controller for DC-DC converters, namely, digital redesign (design by emulation) and the direct digital design (DDC). The digital redesign method suffers from sampling and quantization errors, computational time delay and discretization effects. The direct digital design provides superior performance as demonstrated in [8].

This paper presents, a direct digital control (DDC) method for designing a DSP based dual loop voltage control for a high power fuel cell boost converter, where the RTW is used for automatic code generation for a TMS320F2808 DSP. The PI control law with ant-windup correction is used for the dual loop control. The performance the control method is verified by computer simulations and an experimental setup of a 20 kW boost converter with resistive load during reference voltage changes, input voltage changes, and load disturbances. Obtained results show excellent reference tracking and disturbance rejection properties validating the desired functionality of the proposed controller.

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II. BOOST CONVERTER'S SMALL-SIGNAL MODEL

Linear controllers for DC-DC converters are often designed based on mathematical models. To achieve a certain performance objective, an accurate model is essential. A number of ac equivalent circuit modeling techniques have appeared in the literature [9,10]. Among these methods, the state space averaged modeling is most widely used to model DC-DC converters. The duty cycle to output voltage and duty cycle to inductor current small signal transfer functions of a boost converter with resistive load, shown in Fig. 2, are given by:

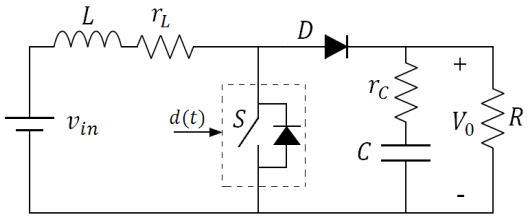


Fig. 2 DC-DC Boost converter circuit

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = G_{dv}\frac{\left(1+\frac{s}{\omega_{zv1}}\right)\left(1-\frac{s}{\omega_{zv2}}\right)}{\Delta(s)} \quad (1)$$

$$\frac{\hat{\imath}_L(s)}{\hat{d}(s)} = G_{di}\frac{\left(1+\frac{s}{\omega_{zi}}\right)}{\Delta(s)} \quad (2)$$

where

$$G_{dv} = \frac{v_{in}}{(1-D)^2} \quad (3)$$

$$\omega_{zv1} = \frac{1}{r_C C} \quad (4)$$

$$\omega_{zv2} = \frac{(1-D)^2(R-r_L)}{L} \quad (5)$$

$$\Delta(s) = \frac{s^2}{\omega_o^2} + \frac{s}{Q\omega_o} + 1 \quad (6)$$

$$\omega_o = \frac{1}{\sqrt{LC}}\sqrt{\frac{r_L+R(1-D)^2}{R}} \quad (7)$$

$$Q = \frac{\omega_o}{\frac{r_L}{L}} + \frac{1}{C(R+r_C)} \quad (8)$$

$$G_{di} = \frac{2v_{in}}{(1-D)^3} \quad (9)$$

$$\omega_{zi} = \frac{1}{C(\frac{R}{2}+r_C)} \quad (10)$$

The transfer function (1) is a second order system with a double pole with corner frequency, given by (7), RHP zero given by (5) and ESR zero given by (4). The angular corner frequency ω_o and right half plane zero ω_{zv2} are functions of nominal duty cycle D. In a closed loop voltage control system, the system elements will change as the duty cycle changes, which means the transfer function will change accordingly. The boost converter under feedback control is a nonlinear function of the duty cycle, which makes controller design for the boost converter much more challenging from the viewpoint of stability and bandwidth [11].

III. DESIGN OF BOOST CONVERTER ELEMENTS

The fuel cells voltage (and power) is determined by two main factors. First the rate at which hydrogen flows through the fuel cell establishes the shape of the V-I polarization curve, as shown in Fig. 3. Second the amount of current drawn by the

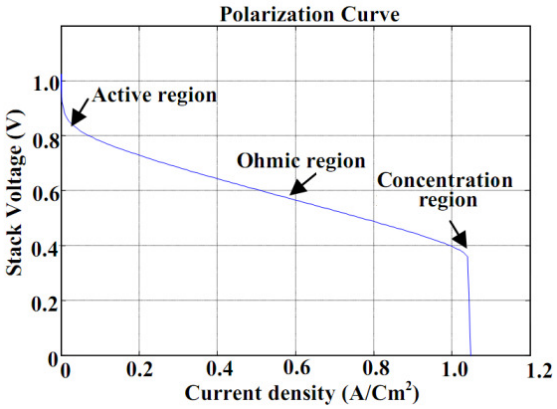


Fig. 3 I-V Characteristics curve of PEM fuel cell single stack

converter determines the point on this curve where the fuel cell will operate. Thus, by controlling the amount of current drawn by the converter, the fuel cell power can be controlled. Therefore for converter design, a linear region (ohmic region) operation of the fuel cell stack is only taken into account. Beyond the linear region, the fuel cells cannot be operated as electrolyte membrane of the cell may get damaged.

The input inductors L and output capacitor C deeply affect the current ripple depression and output voltage performance, respectively. The boost converter is designed to operate in continuous conduction mode (CCM) all the time. Therefore, the minimum output current $I_{o_{min}}$, determines the minimum inductance of the input inductors L as [12, 13]:

$$L_{min} = \frac{D(1-D)^2V_0}{2F_S I_{o_{min}}} \quad (11)$$

where F_s is the switching frequency, D is the duty ratio, and V_0 is the average output voltage. The primary criterion for selecting the output capacitor is its capacitance and equivalent series resistance, ESR, low ESR capacitors will be used for higher efficiency. The output capacitance is chosen to meet an output voltage ripple specifications. An approximate expression for the required capacitance is given by:

$$C_{min} = \frac{V_0 D}{F_S \Delta V_0 R} \quad (12)$$

where R is the equivalent load resistance.

IV. Principle of The Closed-Loop Control Strategies

There are two approaches to design a digital controller for DC-DC converters, they are illustrated namely, the design by emulation or digital redesign and the direct digital design (DDC). Although digital control offers many advantages to DC-DC power converters, its adoption into industry applications has met reluctance from power electronics engineers. The decreasing cost of silicon implementation effective allows digital control to become more cost feasible; however, one factor that continues to inhibit digital control use is the engineers' unwillingness to design control compensators in the digital domain. Typically, power electronics' engineers feel more comfortable designing controllers using traditional analog techniques (e.g., pole/zero placement using bode diagrams). Therefore, digital redesign of the compensator is a popular technique as it requires minimal design in the z-domain.

By using digital redesign method, a linear compensator is devised in the s-domain using traditional design methods. Using one of a variety of discretization methods such as: backward Euler, bilinear and pole/zero matching, the continuous s-domain transfer function can be easily mapped to the z-domain. Although the backward Euler method and the pole/zero matching method produce simpler transfer functions in the z-domain, the bilinear method provides the truest transformation as it preserves the gain and phase of the analog transfer function up to approximately one-tenth of the sampling frequency.

Although digital redesign is capable of providing a good response, it suffers due to discretization effects (such as frequency warping using the bilinear method) and it's disregarded for acquisition, computation, and zero order hold (ZOH) delays which introduces a time delay of $T_s/2$ and a phase delay of $180f/f_s$ where f is the frequency of the bandwidth of the control loop. It is demonstrated in [8] that direct digital design provides superior performance.

In this paper, a dual loop (voltage and current) voltage control is designed using direct digital control (DDC) method and implemented using DSP, as is explained in the following sections.

a. Digital Controller Design

In direct digital design approach, the continuous time power stage model is first discretized with zero order hold (ZOH). Once this is available, the digital controller $G_c(z)$ is designed directly in the z-domain using methods similar to the continuous time frequency response methods. This has the advantage that the poles and zeros of the digital controllers are located directly, resulting in a better load transient response, as well as better phase margin and bandwidth for the closed loop power converter.

Fig. 4 shows the entire closed loop system containing the voltage loop controller $G_{cv}(z)$, current loop controller $G_{ci}(z)$, the ZOH and computational delay, $z^{-\frac{T_d}{T_s}}$, and the control to output transfer functions, $G_{vd}(s)$ and $G_{id}(s)$. The discrete time transfer functions $G_{vd}(z)$ and $G_{id}(z)$of the converter, including the ZOH and the computation delay $e^{-T_d s}$, are given by:

$$G_{vd}(z) = Z\left\{\frac{1-e^{-T_s s}}{s}\cdot e^{-T_d s}\cdot G_{vd}(s)\right\}$$
$$G_{id}(z) = Z\left\{\frac{1-e^{-T_s s}}{s}\cdot e^{-T_d s}\cdot G_{id}(s)\right\} \quad (13)$$

The loop gains for inner current loop and outer voltage loop can be expressed as,

$$T_i(z) = G_{ci}(z)\cdot G_{id}(z)$$
$$T_v(z) = \frac{G_{cv}(z)\cdot G_{ci}(z)\cdot G_{vd}(z)}{1+T_i(z)} \quad (14)$$

The typically adopted controller structure for DC-DC converters is the proportional integral (PI). There is normally no reason to consider more sophisticated approaches, as stated in [5]. In this paper, a digital PI controller will be designed based on the required phase margin ϕ_m and critical frequency ω_{wc} using bode diagram of discrete time systems in w-domain, as explained in [14], the transfer function of the digital PI controller in w-domain is given by,

$$G_c(w) = k_p + \frac{k_i}{w} \quad (15)$$

where

$$k_p = \frac{\cos\theta}{|G_p(j\omega_{wc})|}$$
$$k_i = \frac{-\sin\theta\cdot\omega_{wc}}{|G_p(j\omega_{wc})|} \quad (16)$$

And

$$\theta = 180^\circ + \phi_m - \angle G_p(j\omega_{wc}) \quad (17)$$

By using Euler method, the corresponding z-domain PI transfer function is given by,

$$G_c(z) = k_p + \frac{k_i T_s z}{z-1} \quad (18)$$

Fig. 5(a, b) shows the bode plots for the current loop and voltage loop gains, with the system parameters in table I. The plots indicate that the current loop gain has a crossover frequency as high as 1.2 kHz, with a phase margin of 45°. To accommodate the slow fuel cell response, low control bandwidth is used for voltage loop. The resulting outer voltage loop has a crossover frequency of 40 Hz and a phase margin of 40°.

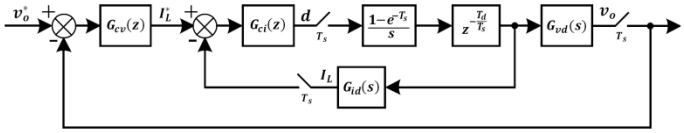


Fig. 4 Dual loop structure

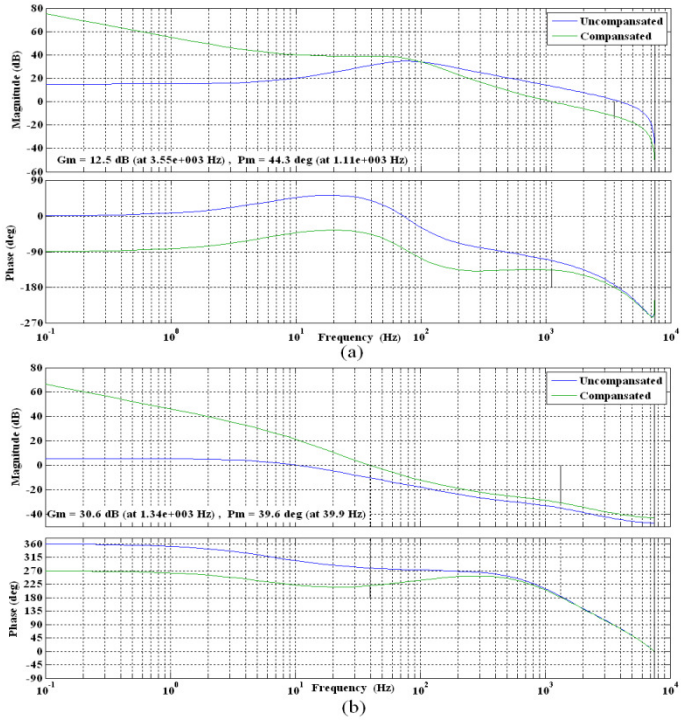


Fig. 5 Frequency response; (a) current and (b) voltage loop gains

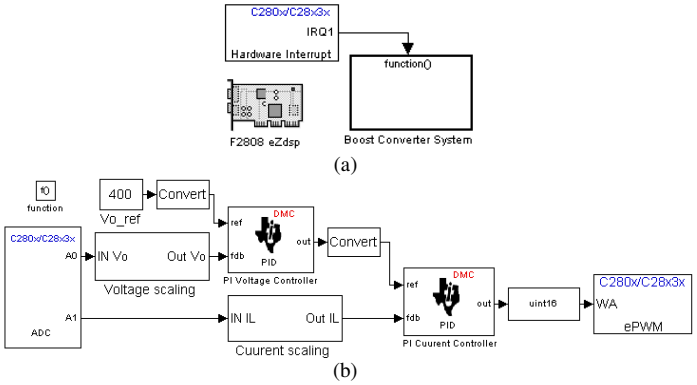
Table I Parameters of the experimental setup

Input voltage, v_{in}	150 V
Output voltage, v_o	400 V
Boost inductor, L	130 μH
Boost capacitor, C	4700 μF
ESR of capacitor, r_C	18 mΩ
ESR of inductor, r_L	75 mΩ
Nominal load resistor, R	10 Ω
Input filter inductor, L_f	10 mH
Input filter capacitor, C_f	42.3 mF
Switching frequency, F_s	15 kHz

b. Controller Implementation

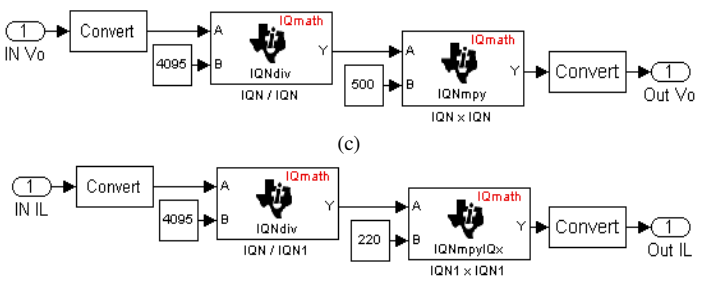
Using MATLAB and Simulink for modeling, analysis, design and offline simulation has become a standard for control system development. The Simulink model is constructed from blocks of the C2000 Embedded Target Library which are used to represent algorithms and peripherals specific to the C2800 DSP family. The Simulink model of the control algorithm is presented in Fig.6. Practically, sampling frequency does not need to be higher than the switching frequency, it is costly to have high frequency ADC, so the sampling frequency is the same as the switching frequency. In order to minimize aliasing effects and reconstruction errors, the sampling and switching processes must be synchronized. In this paper, the Interrupt Service Routine (ISR) block is used to maintain the synchronization between the sampling (ADC block) and the switching (PWM block) processes. The ADC conversion is triggered by the PWM block at the Middle of the switching period (to avoid switching noise and to sample the average value per cycle). The ADC generates an interrupt at the end of conversion, this interrupt triggers the execution of the controller block, as shown in Fig. 6-a. This synchronization process is described in Fig. 7. From Fig. 7 , it is clear that the time delay T_d, between the ADC sampling instant and the PWM duty ratio update, is half the PWM period. In this case, the PWM period and the sampling period (T_S) are equal and so the computation delay is, $T_d = T_s/2$.

A Target Preference block, the F2808 eZdsp block, has to be added to the model. It does not connect to any other blocks, but stands alone to set the target preferences for the model. This allows the user to control build options for the compiler, assembler and linker who will be invoked to generate the executable image file for download to the DSP, as shown in Fig. 6-a. Figure 6-b, shows the details of the boost converter system block, the ADC block samples the output voltage and the inductor current sequentially, these signals are scaled to obtain the actual values, as shown in Fig. 6-c,d . The first signal is compared with the reference voltage value to produce the inductor reference current by a PI controller with ant-windup correction to limit the reference current. This reference current is compared by the current signal to produced the duty ratio by a second PI controller with anti-windup correction to limit the duty ratio. The parameters of the two controllers are calculated in the previous section. The frequency of PWM block is 15 kHz with symmetrical carrier signal.



(a)

(b)



(c)

(d)

Fig. 6 Simulink model that is used to build the code for the TMS320F2808 DSP.

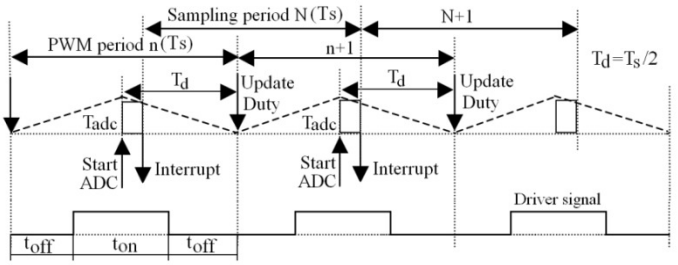


Fig. 7 Boost converter digital control loop sampling and synchronization scheme

V. SIMULATION RESULTS

The proposed control algorithm has been initially tested by MATLAB simulation, the Simulink model is shown in Fig. 8. The converter parameters are reported in Table I. Fig. 9-a shows the system response for step down and up of the reference voltage between 400 and 200 V, Fig. 9-b shows the system response for decreasing and increasing the load with 40% of the rated load, and Fig. 9-c shows the system response for input voltage step down and up between 150 and 130 V. Simulation results verify the efficacy of the proposed controller during different disturbances.

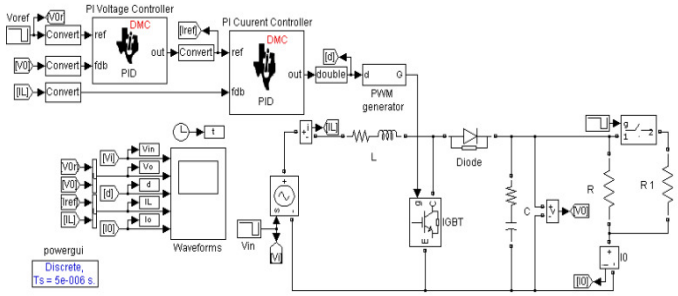
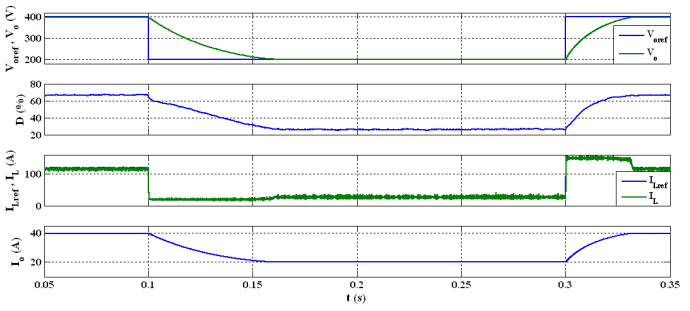


Fig. 8 MATLAB/simulink simulation model



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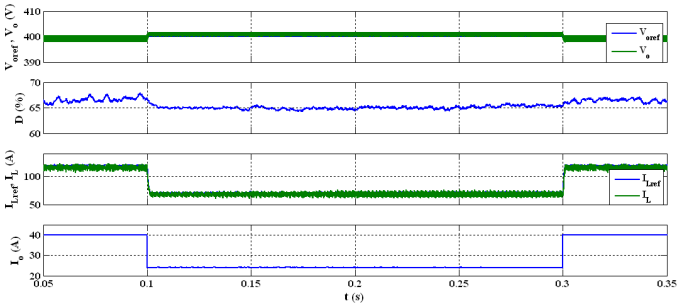

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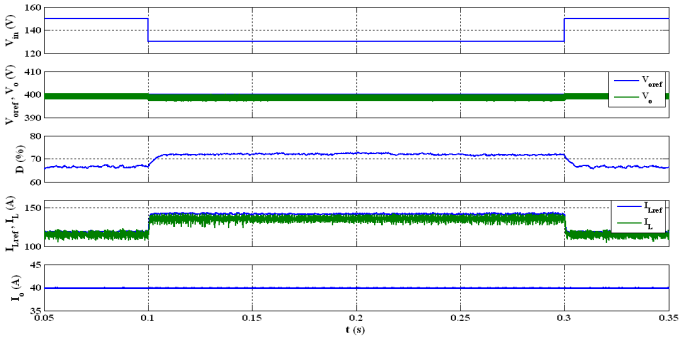
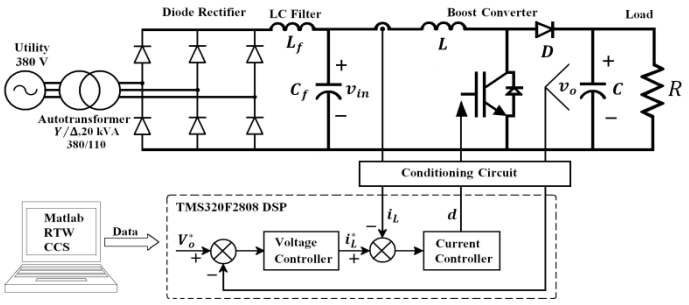


(c)

Fig. 9 Simulation results; (a) reference step up and down response, (b) load step up and down response, (c) input voltage step up and down response



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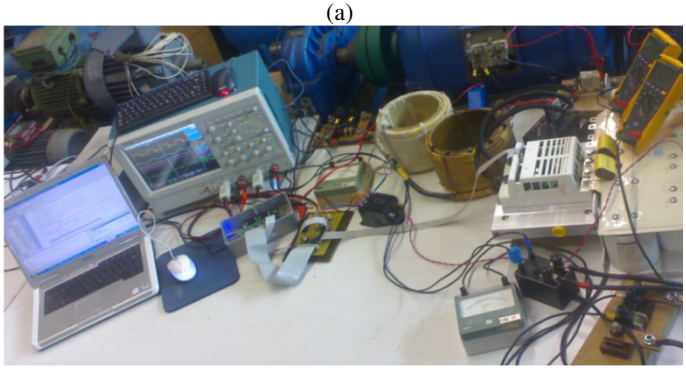


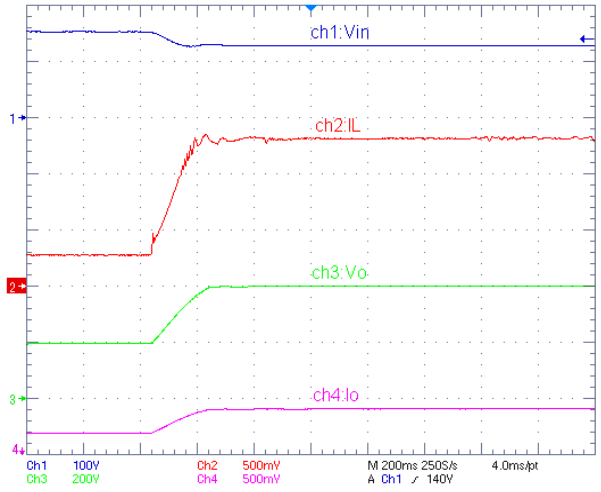
(b)

Fig. 10 Experimental setup of a 20 kW boost converter, (a) Circuit, (b) overview

VI. EXPERIMENTAL RESULTS

The proposed controller has been tested on a 20 kW boost prototype, as shown in Fig. 10, whose converter parameters are reported in Table I. The fuel cell is represented by a DC supply v_{in}. The DC voltage is obtained from the three-phase AC supply through a secondary autotransformer (Y/Δ) connected to a three-phase rectifier bridge followed by *LC* filter. In the above experimental setup, the used boost coil is an air cored coil. A SKiiP 642GB120-208CTV which is 2-pack with integrated gate driver is used for boost converter power electronics elements. LEM sensors are used for output voltage and inductor current sensing. A tektronix oscilloscope is used for signal recording. The eZdsp™ F2808 is used for realization implementation. A conditioning circuit is designed as interface between the DSP and the boost converter.

Fig. 11-a, shows the system response for step-up the reference voltage from 200 to 400 V. Fig. 11-b, shows the system response for step-down the reference voltage from 400 to 200 V. Fig. 11-c, shows the system response for decreasing and increasing the load with 40% of the rated load. Fig. 11-d, shows the system response for input voltage step-down, this test is done at 80% of the rated load to protect the input supply from over rated current. Fig 11-e, shows the steady state waveforms for switching signal, inductor current, input and output voltages. Fig. 11-f, shows experimental system efficiency curve, which indicates that the whole efficiency is about 95~98%, and the efficiency is over 96 % when the output power is large than the half of the rated power.



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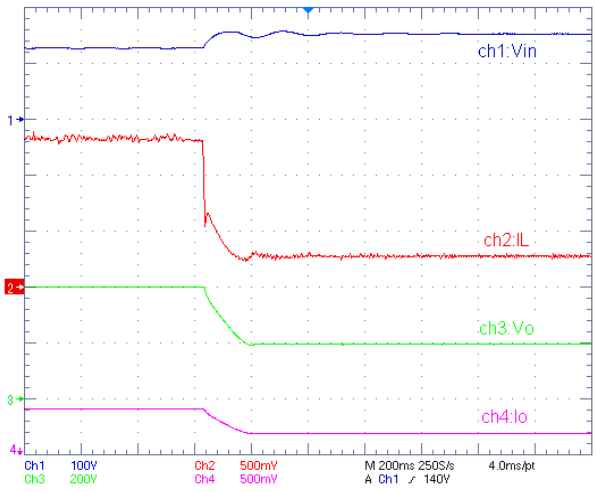

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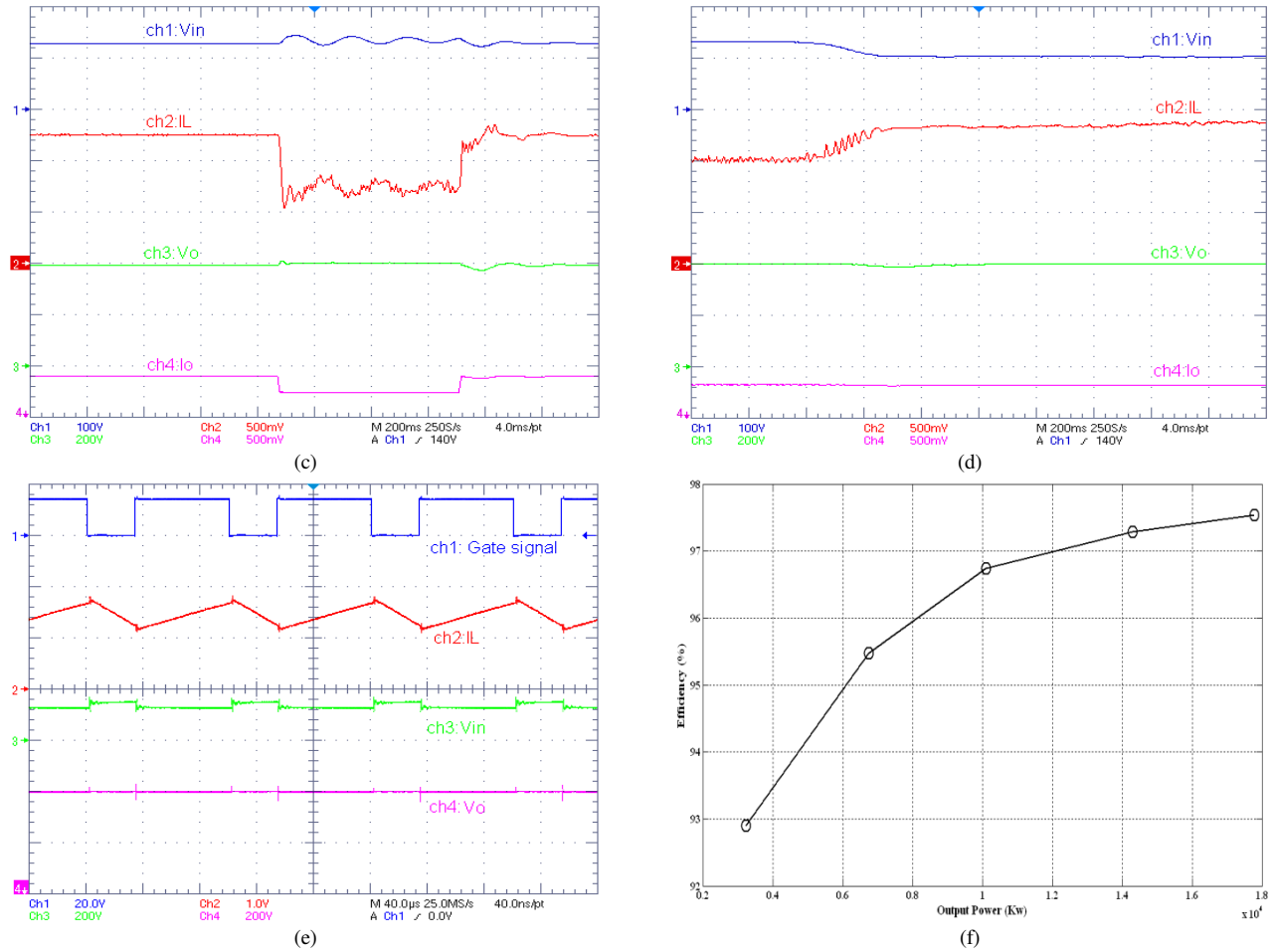

Fig. 11 (a) Experimental results; (a): Reference step-up response, (b) Reference step-down response, (c) Load decreasing and increasing by 40% response, (d) Input voltage step-down response, (e) steady-state waveforms and (f) experimental system efficiency curve.

VII. CONCLUSION

This paper presents a direct digital control (DDC) method for designing a dual loop voltage control of a 20 kW boost converter. The PI control law with anti-windup correction is used for both loops and designed using bode diagram to achieve the required phase margin and critical frequency. In addition, the using of the RTW with the eZdsp™ F2808 DSP for automatic code generation is presented. Simulation and experimental results of a 20 kW boost converter during reference voltage changes, input voltage changes, and load disturbances confirm the effectiveness of the purposed dual loop control during steady state and transient conditions.

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